2-Dimensional Multi Tunneling effect of PtSi/Porous Si Schottky barrier

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Abstract: We report a multi tunnelling junction characteristic in P-type porous silicon core coated with thin film platinum silicide. Detailed analysis of electron transport in this device admits the existence of a structure like a two-dimensional Multi Tunnelling Junctions (2D-MTJ) clearly originate from the sharp edge of created platinum silicide on porous surface. Furthermore, using SIMON simulator, electrical characteristics of proposed 2D-MTJ that modelled as a set of islands, has been extracted to investigate experimental data curves. In accordance with both studies, same oscillations based on coulomb blockade oscillations were observed. In addition the value of current tends to increase proportionally with temperature and for high drain voltage; the device behaves like a single island Single Electron Tunnelling (SET) junction as the simulation predicts. This is probably due to this fact that multiple tunnelling junctions are electrically enlarged and merged into a single island owing to the high applied drain voltage. Also temperature dependence of the coulomb oscillation as a function of gate voltage offers the possible application of this device up to room treatment without cooling payments in comparison to MTJs.

Keywords: Porous Si; PtSi; Schottky barriers; MTJ; SET; SIMON; Coulomb blockade; Coulomb oscillation

Introduction
Platinum Silicides are of the great interest as low-cost stable materials for solid-state microelectronics with application in IR detection and interconnection. By incorporating platinum into silicon, contact resistance can be reduced up to electrical properties of pure platinum. There is a band bending in Platinum silicide (PtSi) between Pt and Si energy band diagram and a Schottky barrier is formed with 0.25 eV heights [1-4]. Regular PtSi Schottky detectors have been extensively studied and are in common usage for 3–5 µm spectral range at 77K [5-9]. Also some attempts have been conducted to achieve room temperature operability of PtSi and improve its detection range up to 7 µm, using p or n-type porous silicon. But a few studies have analyzed electron transfer mechanism of PtSi layer on porosificated Si substrate [10-14]. Comparable changes of porous surface orientation than mean free pass of the photo-excited carriers can explain wider detection spectral of PtSi/Porous Si and also the small depletion capacitance of this schottky junction presents single electron tunnelling (SET) effect at room temperature.

As an alternative approach, some other non-traditional architecture do the same behaviour as basic room operable SET devices which do not requires extremely challenging in nanofabrication technology, commonly known as multi dot SET. In multi dot SETs, the drain and source terminals are coupled by several islands instead of just one [15-19]. In PtSi/Porous layer, as Si pores’ dimension reaches below sub-micron, one possible model that can be suggested for this structure is a two-dimension multi tunnelling junction.

In this work, we are combining PtSi layer with Porous Si which consists of many nanometric silicon residuals and increases Si band gap energy to investigate the electrical characteristics of PtSi/Porous Si Schottky barriers. We firstly describe experimental processes of the device fabrication. Then in simulation section a new simple schematic model of 2D-MTJ with 4-island will be depicted. In continue, using SIMON simulator, we investigate, the electrical characteristics of produced device and finally inspect similarities between PtSi/PS properties with two-dimensional multi tunneling junction structure such as temperature dependence of the coulomb oscillation as a function of gate voltage in the temperature range from T = 5 to 70 K for both studies and compare them with original SETs.

Experimental
The starting material was P-type Si (100) with a resistivity in 17–33 Ω cm range. After RCA cleaning, electrochemical prosification is accomplished by using an electrochemical cell which is a Teflon beaker that Si wafer is placed on a metal disk and sealed through an O-ring, so that only the front side of the sample is exposed to the electrolyte with 40%HF-C2H5OH-H2O solution in ratio of 1:2:1 at constant current density of 30mA/cm² for 15 minutes. 100 Å of platinum is then deposited on the porous Si surface, using e-beam evaporation to observe the best conducting transition on thin PtSi film [27, 28]. The deposited layer was then annealed at 450 °C for 30 minutes. It forms a new phase of material at the interface of platinum and Si. Pt reacts with Si, creating a thin platinum silicides layer over the pores’ peak [Fig.1]. Some unreacted Pt remains inside the pores, which is then etched away in aqua regia and finally an array of metal (i.e., platinum silicide) on semiconductor with different
band gap energy is constructed. To make contact to the silicide surface, 6 µm of molybdenum is deposited on the surface using e-beam evaporation (10^{-7} Torr). Passivation layer was provided by evaporation 10 µm of SiO and SiO2. 6 µm of Al is then thermally evaporated on the formed surface followed by 20 minutes of annealing at 200 °C. Molybdenum is also used as blocking barrier layer for stopping the diffusion of Al into the underlying substrate. Fig 1. explicates the structure used in this study which consists of 3 terminals and SEM image along the device. By applying a reverse bias to source (drain grounded), current flow throw PtSi layer. Changing gate voltage from zero to positive one, initiates 2D-MTJ behaviours. After device fabrication, I-V measurements were made at 77 and 300 K temperature using a HP4145B semiconductor parameter analyzer.

Fig. 1. The cross-sectional structure and SEM of PtSi/Porous Si MTJ and interior used in this study.

AFM profile is taken from PtSi/PS sample shown in Figures 2. The curve in the right side of this figure shows the height of the porous nanowires in the Y axis as a function thickness for a side sliced view of the structure. Phase shifting over pores admit existence of metallic PtSi islands on each pore that forms many potential barriers.

Fig. 2. AFM schematic diagram of PtSi/Porous Si MTJ and height profile along the selected line in sample.

Simulation Section
In PtSi/PS layer, carriers collect on the peak of pores and under a reverse bias, depletion layer of PtSi/PS schottky diode increase. Therefore a set of PtSi islands remain on this layer that can interpret as tunnelling junctions, which transport electrons individually between PtSi islands and the batch of these tunnelling barriers play the role of a 2D-MTJ. Here a Square MTJ as an extension for multi tunnelling junction devices using PtSi/Porous Si Schottky barrier is modelled as a network of resistors and capacitors to explain the behaviour of a finite element 2D-MTJ [Fig. 3]. The number of electrons on each dot is N11, N12, N21 and N22. Each dot is capacitively coupled to gate voltage (Vg) through a capacitor (Cg) and to the source (S) or drain (D) contact through a tunnel junction represented by a resistor R and a capacitor Cm in parallel. We assume dots are coupled to each other by a same tunnelling barrier stand for a resistor Rm and a capacitor Cm in parallel. The bias voltage, Vs, is applied to the drain contact with the source contact grounded (asymmetric bias). Suppose cross-capacitances, other voltage sources and stray capacitances are negligible. Using SIMON 2.0 simulator, a same structure for 10x10, 30x30, 50x50 and 70x70 array of islands simulated to investigate the electrical characteristics of PtSi dots on Porous Si structure. Electrical properties of annullid silicide at the pores’ peak, is maintained and a high density tunnelling junction structure will compose between these pores in porous Si (PS). The main advantages of 2D-MTJs in comparison to single-island single electron tunnelling junction with identical dimensions of islands and tunnelling junctions are a higher threshold voltage of Coulomb blockade and, as a consequence, a higher operation temperature [20-26].

Fig. 3. Network of resistors and capacitors representing Square MTJ.

Results and Discussion

1) Bias voltage and polarization
Fig. 4. shows the absolute value of drain current Id as a function of the gate voltage Vg for both under study sample at 77K and simulated 10x10 array of tunnelling junctions at 5K. We use only one polarization source ‘Vd’ because we choose the source potential at zero. By increasing gate voltage, depletion layer of PtSi/PS schottky diode extends into Porous Si region and consequently carriers transfer into the source is interrupted by tunnelling numbers. For a high applied drain voltage, the 2D-MTJ behaves as a single island SET. This is probably because the islands are electrically enlarged and merged into a single island owing to the high applied drain voltage. The height of tunnel barriers is lowered at a high Vd. Owing to the various barrier
heights in the devices; the Fermi level of the electrode exceeds the height of one of the tunnel barriers at a certain Vd. Thus, the device effectively behaves as a one-island device. Comparing the Id–Vgs characteristics of two figures in a. and b. at different Vd, remark us ordered increase in PtSi/Ps current value due to its huge number of tunnelling elements carried out carriers transform.

2) Temperature dependence
The Id–Vg characteristic for 10x10 array of tunnelling junctions is presented in Fig. 5.a. We note that, for this array, there are two picks at low temperature, and at higher temperature, smaller peaks disappeared and only one major peak at the same value supply stands [Fig. 5.b]. The temperature depends on Id at the peaks and it is observed that the value of central peak increases with increasing temperature value. For large temperature, our structure tends to a structure with an island.

3) Increasing tunnelling junctions
Adding the number of junctions in the MTJs is often motivated by the necessity to increase the Coulomb energy of the system and to reduce spontaneous cotunneling events.

These events, which are the higher-order processes, are associated with electron tunnelling occurring in several junctions simultaneously and quantum-coherently. In order to make these devices more accurate and reliable, the number of series-connected junctions should be increased in two directions. Their main advantages in comparison to single tunnelling junctions with identical dimensions of islands are a higher threshold voltage of Coulomb blockade [Fig. 6] and, as a consequence, a higher operation temperature. To make sure that the current increases with elements’ number in 2D-MTJs, Fig. 7 will be used. It describes the characteristics for large 2D-MTJs to estimate experimental data, respectively, for 10x10, 20x20, 30x30, 50x50 and 70x70 island of tunnelling junction simulated at T = 5K and...
Vd=0.03v. Because, the simulation time highly intensified by elements order it couldn't process larger ones. Our simulated result resembles the experimental data at low temperature, but the experimental data is larger than the modelled data with large current value and has less asymmetry. The discrepancy can be resulted from several approximations in our simulations, including that there is not always same tunnelling barriers and capacitance and resistance for each pore pair due to prosification procedure. Also cross-tunneling was not taken into account in the present model.

Conclusions
Using PtSi on porous Si we fabricated a two-dimensional multi tunneling junction and by applying SIMON simulator, we investigate the electrical characteristics of modeled device and show the temperature dependence of the coulomb oscillation of the 2D-MTJs as a function of gate voltage Vg in the temperature range from T =5 to 70K. In conclusion, current value tends to increase as temperature increases and for a high drain voltage, the 2D-MTJ behaved as a single-island single electron tunneling junction. It follows output I-V characteristics of fabricated device by extending model elements. This approach may be used to provide a simple fabrication method for 2D-MTJs used in memory cell's development.

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References


